Notice of Allowability	Application No.	Applicant(s)	
	09/854,038	GRUPP ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *5 July 2005*.

2. ☒ The allowed claim(s) is/are *3,5,13,14,16,18,19,21,26,28-31,33,35,37,40,42,45 and 47 now renumbered as claims 1-24*.

3. ☒ The drawings filed on *11 May 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *7/8/05* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

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DETAILED ACTION

1. Amended independent claims 3, 5, 13-14, 16, 18-19, 21, 26, 28-33, 35, 37, 40, 42-43, 45, 47 and 48 are currently pending in this application based on applicant's amendment filed 5th July 2005.
2. Claims 12, 20, 22, 34, 36, 39, 41, 44 and 46 are cancelled by the amendment.
3. Claims 37, 42 and 47 are written in an independent format by the amendment submitted on 5th July 2005. Claims 3, 5, 13-14, 16, 18-19, 21, 26, 28-31, 33, 35, 37, 40, 42, 45 and 47 are amended.
4. Claim 37 however was not written in an independent format to contain all limitation of preceding & independent claims. Claim 37 dependence hierarchy contained claim 36, 34 and 12 (independent claim), but the amended claim 37 had claim 36 substituted with claim 35. Further, claim 36 was cancelled; hence the limitation in claim 36 was lost. Further, claim 35 was not cancelled and amended to depend from claim 37, whereby repeating the limitation. Examiner believes this was an oversight and has entered an examiner's amendment after an interview with the attorney of record (See Examiners Amendment for details).
5. Claims 36, 42 and 47 and depending claims are allowed over the prior art of record, after examiner's amendment.
6. Claims 3(3), 5(4), 13-14(5-6), 16(7), 18-19(11-12), 21(13), 26(17), 28-33(18-23), 35(8), 37(1), 40(14), 42-43(9-10), 45(24) and 47-48(15-16) are renumbered as shown in parenthesis next to them.

EXAMINER'S AMENDMENT

7. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Jim Syta (Registration # 50949 at Schmeiser, Olsen & Watts) on 28th July 2005 at 10:40 am.

Amend claim 37 with the following:

In claim 37, lines 23-24 please **delete** "wherein the control mechanism used HDL register values to detect the change on both the first port and the second port," and **insert** "wherein the gates of the third and the forth NMOS devices are held high throughout the computer simulation of the electronic device,".

Further, **delete** period on line 9 and **insert** a semicolon. The amended claim should now read as follows (examiners amendment bolded and underlined):

> 37. (Currently amended) A model for representing a bi-directional wire input/output (I/0) during computer simulation of an electronic device, the model being tangibly embodied in a computer readable memory unit that comprises a Hardware Description language (HDL) application program therein, the model being adapted to be used in a computer simulation of an electronic device by executing the HDL application program on a processor of a computer system, the model comprising:
> a) a first path between a first port and a second port, the first path including a second NMOS device**[[.]] ;**
> b) a second path between the second port and the first port, the second path including a first NMOS device; and
> c) a control mechanism, the control mechanism checking signal values (S1) on the first port and signal values (S2) on the second port when a change is detected on the first port or the second port, the control mechanism enabling the second NMOS device when a change is detected on the first port and the first port does not equal to the second port, the control mechanism enabling the first NMOS device when a change is detected on the second port and the first port does not equal to the second port, wherein the second path further includes a third NMOS device and wherein the first path further includes a forth NMOS device, wherein the third and forth NMOS

devices are tied on to function as pass devices, wherein the first path and second path are electrically in parallel, wherein the second NMOS device and the forth NMOS device are electrically in series within the first path, wherein the first NMOS device and the third NMOS device are electrically in series within the second path, **[[wherein the control mechanism used HDL register values to detect the change on both the first port and the second port,]]** **wherein the gates of the third and the forth NMOS devices are held high throughout the computer simulation of the electronic device,** wherein the control mechanism comprises a first control output C1 directly coupled to the gate of the first NMOS device and a second control output C2 directly coupled to the gate of the second NMOS device, wherein the signal values (S1) at the first port are directly coupled to a source/drain of the first NMOS device, and wherein the signal values (S2) at the second port are directly coupled to a source/drain of the second NMOS device.

Allowable Subject Matter

8. Claims 36, 42 and 47 have now been allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance:

Applicants are disclosing a model and a method for representing a bi-directional wire input/output (I/O) during a computer simulation, where the two ports are connected with two paths in parallel, each path containing two NMOS devices each, one of each NMOS device on each path acts as an pass device where gate held high during simulation, and the second NMOS device on each path is controlled by a ***control block*** such that only one path is enabled any one time. The ***control block*** senses the change on the two ports of the bi-directional wire model and compares them to generate the control signals to turn the *second NMOS devices* on each path, hence enabling the paths. The unique feature of this disclosure is the exact arrangement of the four NMOS devices and the ***control block*** between the two ports of bi-directional wire model as presented by the disclosure. The individual steps of defining the two paths in parallel comprising NMOS devices each in series, enabling the paths based on change in a signal values at the two ports using control block (mechanism) have been disclosed in prior art of record.

Specifically, such model features are taught by U.S. Patents 5,202,593 (Huang), 6,496,955 (Chandra), and 5,396,435 (Ginetti) individually or in combination.

While these features are individually disclosed in the prior art, the prior art of record does not meet the conditions as suggested in MPEP section 2132, namely:

"The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an **ipsissimis verbis** test, i.e., identity of terminology is not required. **In re Bond**, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

In particular, the prior art of record does not disclose connecting drain/source of the first NMOS (See Fig.2: A1 or A2) on any one of the paths to the input/output ports (See Fig.2: PORT_A or PORT_B) and gate of the first NMOS to the control block through the selective drive signals (See Fig.2: C1 or C2) in implementing a bi-directional wire I/O model (See Specification: Pg.12 Lines 14-21; Pg.13 Lines 1-11). Further, the control block implementation is limited to the generic sensing implementation disclosed (See Fig.3, 5-6) in the Verilog/VHDL models and behavior disclosure (See Specification: Pg.14 Lines 7-13).

The closest prior art uncovered during examination teaches certain limitations of the claimed invention as follows:

U.S. Patents 5,202,593 (Huang): Huang '593 discloses in Fig.1, a first path (element 13) between first port (element 12) and second port (element 14). Further, Huang '593 discloses in Fig.1, a second path (element 11) between second port (element 14) and first port (element 12).

Huang '593 also discloses a buffer, a three-input NOR-gate and a single-shot device (Huang '593: Col. 2-Line54-56). NOR gate and a single-shot device act as control mechanism (Huang '593: Col. 1-Line 20-22). The control mechanism senses the

change between the ports (Huang '593: Fig.1-Element 12 & 14) with corresponding to signals S1 and S2 and drives the second port with the same input signal as the first port (Huang '593: Col. 2-Line 28-37). The control mechanism also enable the appropriate path by disabling the second path until the driving signal is asserted on the first port (Huang '593: Col. 2-Line 38-47), hence only one path is driving the ports at any given time. The same reasoning works when the signal is asserted on the second port and it drives the first port. Further, Claim 12 is rejected as Huang '593 teaches a buffer (Huang '593: Fig. 2), which is a pass device comprising of NMOS devices (conventional symbol). Teaching of Huang '593 are disclosed in claim 35 rejections above. Huang does not explicitly teach holding the gates of third and forth NMOS devices high. Holding the gates high on third and forth NMOS devices is equivalent to having a wire/short between the drain & source, rendering them futile as far as signal control. From the delay-modeling perspective, Huang '593 also uses transistor devices and delay can be modeled in his transistors using the same process as provided in specification. Huang '593 does not disclose that circuit is a *model for representing a bidirectional wire* [bus] *input/output (I/0) during computer simulation.* Further, Huang does not teach that the control block enables NMOS devices by selectively applying signals to the gates of the NMOS devices, now recited in the independent claims 37, 42 and 47.

U.S. Patents 6,496,955 (Chandra): Chandra teaches us that a module can be represented in high-level HDLs such as Verilog hardware description language (HDL) or VHDL written in RTL or transistor level using primitives provided by HDL

(Col. 4-Line 7-20). Verilog or VHDL module is a model of actual circuit that can be executed on a computer and Chandra teaches us how create such a module (Col. 4-Line 21-44, Line 60-67) by example. Although Chandra teaches modeling, it does not teach the exact circuit disclosed by the disclosure as claimed by the Fig.2.

U.S. Patents 5,396,435 (Ginetti): Ginetti teaches that timing path delay values at an input port of a primitive cell is represented by a capacitance (Ginetti '435: Col. 2-Line 35-55). The model/method of the bi-directional wire in applicant's disclosure is concerned with the delays which Ginetti teaches, however Ginetti does not teach the control block which enables NMOS devices by selectively applying signals to the gates of the NMOS devices, now recited in the independent claims 37, 42 and 47. Further, it does not teach the exact circuit disclosed by the disclosure as claimed by the Fig.2.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled **"Comments on Statement of Reasons for Allowance."**

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R. Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Tuesday, July 26, 2005

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